

REMARKS

Claims 1, 3, 13, 15-18 and 21 are pending. Claims 1 and 13 have been amended.

Claim Rejections - 35 U.S.C. § 101

The Patent Office rejected claims 4, 6-9, 11, 12, 19 and 20 under 35 U.S.C. § 101 for failing to be statutory subject matter.

Applicant respectfully traverses. However, claims 4, 6-9, 11, 12, 19 and 20 have been canceled without prejudice.

Claim Rejections - 35 U.S.C. § 112

The Patent Office rejected claims 13, 15-17 and 18-21 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Applicant respectfully traverses. However, claim 13 has been amended and complies with the written description requirement.

The Patent Office rejected claims 13, 15-17 and 18-21 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Applicant respectfully traverses. However, claim 13 has been amended and complies with the enablement requirement.

The Patent Office rejected claims 13, 15-17 and 18-21 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant respectfully traverses. However, claim 13 has been amended and is definite to a person of ordinary skill in the art.

Claim Rejections - 35 U.S.C. § 103

The Patent Office rejected claims 1, 3-4, 6-9 and 11-12 under 35 U.S.C. § 103(a) as being unpatentable over Fredericks et al., U. S. Patent 4,939,735 (Fredericks) in view of Lay, U. S. Patent 6,862,293 (Lay).

The Patent Office rejected claims 13 and 15-17 under 35 U.S.C. § 103(a) as being unpatentable over Fredericks et al., U. S. Patent 4,939,735 (Fredericks) in view of Si, U.S. Patent 7,010,612 (Si) in further view of Lay, U. S. Patent 6,862,293 (Lay).

Applicant respectfully traverses each rejection under 35 U.S.C. § 103(a). The present application provides a novel apparatus for implementing a single-thread, multiple-speed / multiple-thread, single speed dual-mode interconnect protocol method with shared resources on a single die. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Ryoka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). *See also In re Wilson*, 165 U.S.P.Q. 494 (C.C.P.A. 1970). Applicant respectfully submits that claims 1 and 13 recite elements which have not been disclosed, taught or suggested by Fredericks, Lay and Si, individually or in combination. For example, claim 1 generally recites a first and second circuitry capable of transferring data across at least two interconnect protocol definitions, the at least two interconnect protocol definitions including a single-thread, multiple-speed protocol and a multiple-thread, single-speed protocol method. Claim 13 generally recites means for converting a parallel word into at least one serial differential bit stream, the converting means being disposed on said single die; the converting means including an input selector in which said apparatus operates according to a selected protocol definition, wherein transforming means and converting means are capable of transferring data across at least two interconnect protocol definitions, the at least two interconnect protocol definitions including a single-thread, multiple-speed protocol method.

The Patent Office correctly states that Fredericks fails to disclose an apparatus capable of implementing at least two interconnect protocol definitions, the at least two interconnect protocol definitions including a single-thread, multiple-speed protocol and a

multiple-thread, single-speed protocol method as recited in claim 1 and 13. Lay fails to cure the defects of Fredericks. The Patent Office cites Column 7, Lines 29-31 for support of its assertion that Lay discloses an apparatus capable of implementing at least two interconnect protocol definitions, the at least two interconnect protocol definitions including a single-thread, multiple-speed protocol and a multiple-thread, single-speed protocol method. However, this passage merely describes an interconnect apparatus which converts 1G or 2G data transfer link to a 10G data transfer link or a 10G data transfer link to a 1G or 2G data transfer link. (Lay, Column 7, Lines 36-39). An interconnect apparatus which converts a 10G data transfer link to a 1G data transfer link is not equivalent to an apparatus, located on a single die, capable of transferring data across a single-thread, multiple-speed protocol method and a multiple-thread, single-speed protocol method. In fact, Lay fails to even recite the terms single-thread, multiple-speed protocol method and a multiple-thread, single-speed protocol method. Thus, under *in re Ryoka*, a *prima facie* case of obviousness has not been established for claims 1 and 13. Claims 1 and 13 should be allowed. Claims 3, 15-18 and 21 are believed allowable due to their dependence upon an allowable base claim.

Additionally, claim 13 recites an input selector. The Patent Office correctly states that Fredericks and Lay fail to disclose an input selector. Si fails to correct the defects of Fredericks and Lay. Si fails to disclose any type of input selector for operating according to a particular protocol. The Patent Office cites Column 3, Lines 48-50 for support of its assertion. However, this passage merely mentions that a receive data circuit is programmable. This is not equivalent to a input selector for operating according to a particular protocol. Thus, another element of claim 13 has not been disclosed, taught, or suggested by Fredericks, Lay and Si. Under *in re Ryoka*, Claim 13 should be allowed.

CONCLUSION

In light of the forgoing amendments, reconsideration of the claims is hereby requested, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

LSI Logic, Inc.

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A handwritten signature in black ink, appearing to read "Chad W. Swantz", written over a horizontal line.

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